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Design of high speed serializer for interchip data communications with phase frequency detector

Vinod Kumar Nirala*, Shalini Chaudhary**, Monika Gupta*
**(Department of Electronics and Communication, Uttarakhand Technical University, Dehradun)*
*** (Department of Electronics and Communication, Beehive College of Engineering & Technology, Dehradun)*

ABSTRACT
The part of project work presented in this report deals with high speed inter-chip serial data transfer. Serializer used for parallel to serial conversion is of not only high speed but also power efficient. The utilization of CMOS based serializer as well as CML (current mode logic) based serializer at proper places helps in reducing the power requirement without compromising the adequate speed. Tree structure is adopted for the realization of higher order serializer(8:1). The basic building block is 2:1 serializer. The high frequency clock is generated with the help of delay locked loop (DLL) based clock multiplier unit (CMU). Pre-charge type phase frequency detector (PFD) is used to obtain better phase resolution which is necessary for enhancing the jitter performance of the transmitter. DLL generates 8 phases which are combined by a logic block to produce a clock of frequency 4 times input frequency of DLL. To obtain different other frequencies divider is utilized.
Keywords **-** CMU, DLL, Logic Block, Pre-charge type PFD, Serializer, VCDL.

I. INTRODUCTION

1.1 Objective

Intra chip communication is faster than inter chip or off- chip communication. The signal processing modules used on the chip is even faster than on-chip communication. Basic reason behind such improvement in performance is enhancement in device performance. Band gap engineering and device scaling basically brought so many desired changes in device properties. All such improvements add to accelerate the speed performance of the signal processing modules. But the inter and intra chip communication does not support such a high speed. The major issue is noises, cross talk, limited channel bandwidth etc. This project targets to minimize these effects and hence enhance the speed of the interfacing circuit. The target is to achieve a speed of 2 Gbps with low jitter and compact design. The project concentrates on the design of a low jitter, wide frequency range serialization unit which produces high speed serial data that is used by precoding module to encode the data and send it through high speed buffer. The technology used is 180nm.

II. LITERATURE SURVEY

The overall system can be divided into three major parts, 1. Transmitter, 2.Channel and 3.Receiver. The project deals with the transmitter section mainly. The major building blocks in the transmitter are serializer, CMU, Precoder and Divider. The serializer is used to serialize the parallel data. The 16 data streams are required to serialize. It is accomplished by the help of two nos. Of 8:1 serializers.Muxes are used as a selector for the different incoming data based on the control signals generated in course of obtaining the serialized output.

System Overview

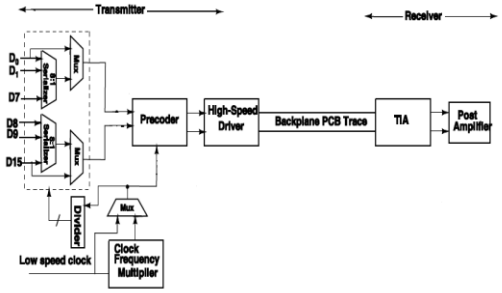

Fig.1: Block Diagram of inter-chip data transfer

The second major unit used is clock multiplier unit (CMU). It converts the low frequency clock into high frequency clock. The present project talks about DLL based CMU. DLL produces the different phases of the same clock and send it to a logic block which combines them to produce high frequency clock. the divider circuit is used to produce lower frequencies required at different stages of the serializer system. 16 input data streams are serialized with the help of CMU and serializer and sent to precoder. Precoder utilizes the multilevel signaling to encode the data. Multilevel signaling is better for the high speed data transfer. The reason is the choice of signaling scheme plays a major role in high speed

data transfer application. There are many encoding schemes like NRZ, duobinary and PAM4 which can be utilized for data transfer at high speed[1]. The scheme which will be considered for this project will be decided later when the things uptoserializer will be completed. The high speed buffer driver is required to minimize the reflections and other channel requirements. As the design of receiver section is not the part of the project, we will not go in depth for this section while explaining the system overview but just for completeness little light on this part is also necessary. The transmission line is generally used as the channel. The offered matching resistance of this transmission line 50 ohm. At the receiver section the reverse work of the serialization is accomplished. Trans impedence amplifier(TIA) is used for receiving purpose. After reception, generally the signal is of very weak strength so it is required to boost its strength. Post amplifier is used increase the strength of the received signal.

III. MOTIVATION

To enhance speed and reduce area the better choice is serial data transfer in place of parallel data transfer. It facilitates the high speed performance for the link and minimizes many unwanted effects. It also allows less complexity in design and routing. The serializer might be of higher order to serialize many parallel inputs but in this project 2:1 serilalizer is used to make higher order serilaizer. The design of lower order serializer needs fewer transistors so it is less complex. The simulation is also easier for such lower order serializer. By using proper clock frequencies at different stages, these lower order serializers are used to realize higher order serializer. The quality of the signal is determined by different aspects like jitter, reflection and clock skew. These aspects plays major role in determining the reliability and performance of a design requiring high speed. The performance of transmitter not only helps the sender section to send proper data but also the receiver finds it easier to recover the clock and data from the incoming data.

The necessity of high speed clock can be fulfilled in two ways, either a very high frequency clock is directly used or low frequency clock is passed through a clock multiplier to have a high frequency clock. The first method is becomes inadequate when the required speed becomes very high (few gigahertz). The second method might be an alternative for the similar purpose. CMU is used to generate high frequency clock. The DLL based CMU is generally used in the industry to get higher speed clock. At high speed, some of the issues come into the picture strongly to achieve high quality performance. The main constraints appear due to limitations of different building blocks of the DLL. Each different unit have different limitations that affect the overall performances .Phase and frequency detector (PFD) imposes the problem of its resolution. The PFD resolution should be high in order to minimize static phase error that helps in reduction of jitter. It reduction in static phase error increases the closed loop speed. The current mismatch in charge pump is greatly affected due to low resolution of the PFD. Hence we find, high resolution is an stringent requirement to achieve high speed in DLL. Generally PFD is realized by conventional method (D flip flop based) but this project used pre-charge type PFD which offers higher resolution[3]. Actually, PFD is closed loop system so the delay of the circuit becomes an important parameter to determine the speed of the same. Delay is also dependent upon swing of the voltages[11]. We will verify this result in the result section of the project. We will see how the larger delay of conventional PFD causes less resolution whereas pre-charge type PFD offers high resolution. Hence it allows less phase offset and overall speed is enhanced to a greater amount. Apart from resolution of DLL, the lock range of voltage controlled delay line (VCDL) is another very important parameter[2]. The high lock range is targeted to achieve in this project.

Along with clock generation, the clock distribution in a complex high performance system has its own problems. Generally, 50% duty cycle is a necessary requirement for precoding and transmitting high speed data. It makes necessary the use of duty cycle correction circuit (DCC). Sometimes buffers are also required in the distribution path of the clock. We will see inverting as well as non-inverting buffers required at different place in course of realization of the circuit.

IV. RESEARCH METHOD

3.1 Serializer

The project utilizes the two nos. of 8:1 serializer two serilaize the 16 incoming parallel streams. The each 8:1 serializer is made of seven nos.of 2:1 serializers.

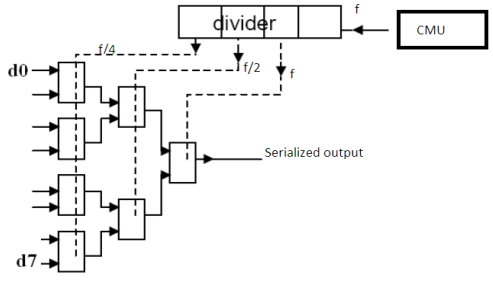

Fig. 2- 8:1 serializer using tree structure of 2:1 serializer

They are arranged in the tree fashion as shown in the fig. 2. The CMU produces 2 Gbps clock which is divided by divider to generate three control signals having frequencies 2 GHz, 1 GHz and 500 MHz. The 2:1 serializers are arranged in 3 stages requiring different Speeds of the clock as shown in fig-2.

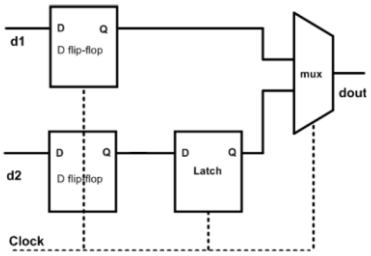

Fig. 3- Building block of 2:1 serializer

3.1.1-2:1 Serializer

Now we concentrate on very basic building block of entire serializer. 2:1 serializer is used in the project to design 8:1 serializer. We can think a multiplexer can do the operation of serialization but practically we don't get the proper serialization. The different timing requirements (set up time, hold time, other types of delay) put stringent limitations on the design. The basic internal blocks are shown in fig-3. Two flip-flops , one latch and one mux are required to design this. The clock fed to each block is same and also the flip-flops and latches both must be either positive edge triggered or negative edge triggered. The latches are basically providing the delays to the incoming signals. The delay must be half of the clock cycle. Generally, clock starts from the middle of the data input. As rising edge of the clock will select one of the data input and this rising edge is in the middle of the selected data input, then the falling edge of the clock will occur exactly at the falling edge of the second data stream. This will cause a problem of synchronization for the second data stream and the clock. It may be when the falling edge of the clock appears, correct data is unavailable in the second data stream. To avoid such problem of erroneous output, one latch is used. It provides the delay which helps in finding the correct data in the second data stream whenever negative edge of the clock appears.

The project includes serializers based on two different concepts- 1. CMOS based serializer and 2. CML based serializer. CMOS architecture of serializer allows full Swing in the output whereas CML design allows reduced swing. The swing affects the speed of the circuit. The CML logic is faster due to reduced swing but it dissipates the huge power[7][8]. The reason is being the transistors in the saturation region.

There is a path between ground and supply all the time which causes a flow of current continuously and it results in higher power consumption. The qualitative and quantitative analysis of these two type of serializers are given in Table-1. The CML logic offers less glitches in comparison to the CMOS logic based serializer[9]. Due to having larger swing the delay becomes larger which causes more glitches. The results are shown below. It will clearly quantify and qualify the performance of these two types of serializers.

Table-1
Comparison of performance

Type of serializer	CMOS	CML
Speed	800MHz	2 GHz
Power consumption	Very less	5.4mW
Error(glitches)	More	Less

Now the question arises, whether CML based serializer should be used (due to higher speed) or CMOS based serializer (due to comparatively negligible power consumption) or both. The presented project will use both of them. It will allow to take the benefit of high speed as well as low power consumption. The final stage of the 8:1 serializer will be designed with 2:1 CML serializer to support high speed at this stage but the rest stages will consist of 2:1 CMOS serializer because at lower stages the speed requirement is not very stringent. Hence the speed as well as power performances can be enhanced. The simulation results are shown on the next pages. We can distinguish the mentioned differences from the simulation results. Fig-4 shows the serialization process of CMOS based serializer whereas the next fig-5 is for CML based serializer. The later offers better speed as well as better quality of the serialized output. The former produces more glitches which are clearly evident from the fig4 and 5

Simulation Results

(1)

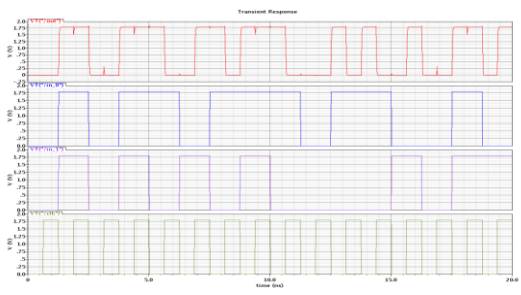

Fig.4- output of 2:1 CMOS Serializer

(2)

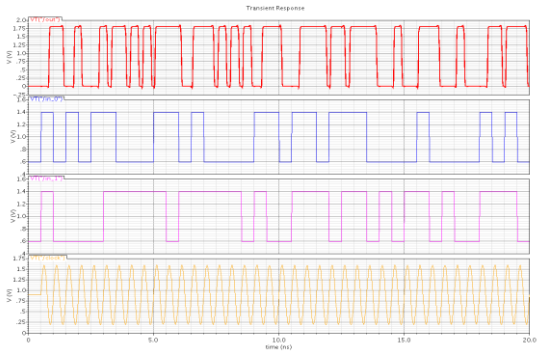

Fig-5- output of 2:1 serializer

3.2 Clock Multiplier Unit(CMU)

The DLL based clock frequency multiplier produces an output clock with frequency four times that of the input clock. The clock is required not only for serialization process but also for precoding process. The block diagram of the DLL based CMU is shown in fig-6. It consists of mainly DLL and Logic block. The DLL unit generates the 2N nos. of phases which are combined by the Logic Block to produce N times higher frequency clock. Multiplexer is basically used to pass the multiplicand. In the present project, N=4 is used, it means 8 nos. of phases will be generated and combined by logic block to output 4 times higher frequency clock.

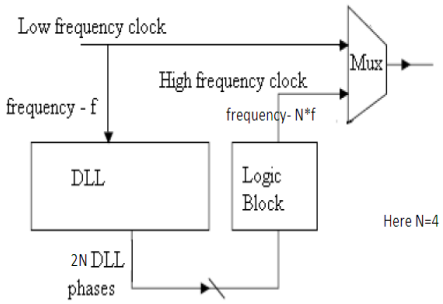

Fig-6 Clock Multiplier Unit (CMU)

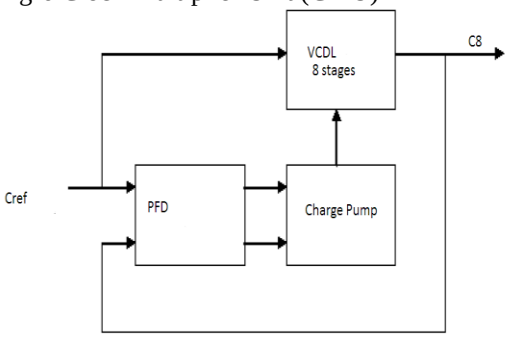

Fig-7. Delay Locked Loop

3.2.1Delay Locked Loop

A delay locked loop is used to synchronise the output of DLL with the input frequency. It provides exactly one time period delay[4]. The block diagram is shown in fig-7. The synchronization of the output of the DLL with the original clock is a very vital requirement for the minimized jitter performance of the transmitter [5]. The output of DLL is compared with the second pulse of the original clock to make sure the phase synchronization and one period delay. As shown in fig-7, DLL consists of three major building blocks- 1.PFD, 2. Charge Pump(CP) and 3. Voltage Controlled Delay Line (VCDL). DLL functions very similar to PLL. But due to easier design procedures and less jitter, it is mostly used in the industry. The performance of PFD is the major contributor in good quality clock generation and to minimize static phase offset in CMU. The high resolution PFD is required to have high performance CMU[3]. CP generates the control voltage required to vary the delay of VCDL. The charging and discharging currents of the CP must be same in order to have minimized static phase offset.

VCDL produces eight phases. The eighth phase is compared with the original clock[8]. The difference in phases is evaluated by PFD and by the help of CP, the control voltage is generated and fed to VCDL. Non-Zero control voltage has been generated unless the locking takes place.

3.2.1.1 Phase and Frequency Detector(PFD)

Generally conventional PFD is utilized for the comparison of phases of two signals. Fig-8 shows the basic building blocks of such PFD. When reference signal leads the output signal of VCDL , UP signal becomes high, in the reverse scenario DN signal becomes high[12]. The resolution of PFD is a very important quantity. It affects many parameters of the whole design. The conventional PFD doesn't show very high degree of resolution. We will see shortly how it does not show good resolution in the result section of PFD. The project includes a different type of PFD which has better resolution. This is based on pre-chrge type of logic family[13]. The delay offered by pre-charge type PFD is lesser than that of conventional PFD. It helps in enhancing the resolution of the circuit. The fig-9 is the transistor diagram of the precharge type PFD. The nos. of transistors required in precharge PFD is less than conventional one[13]. The significant distinction between these two types are the delay provided by the configurations. As second circuit provides less delay it allows faster operation refer fig-10,11.

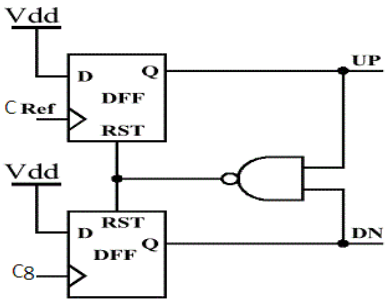

Fig-8- Conventional PFD[13]

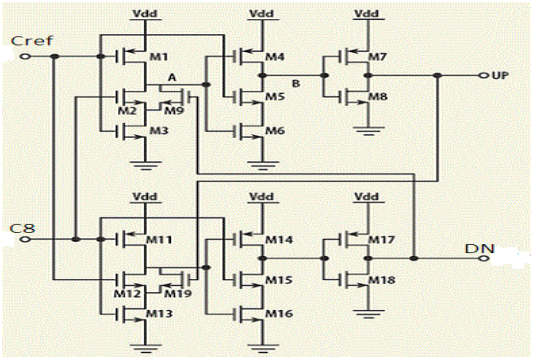

Fig.9- Pre-chrge type PFD[13]

V. RESULTS AND ANALYSIS

(1)

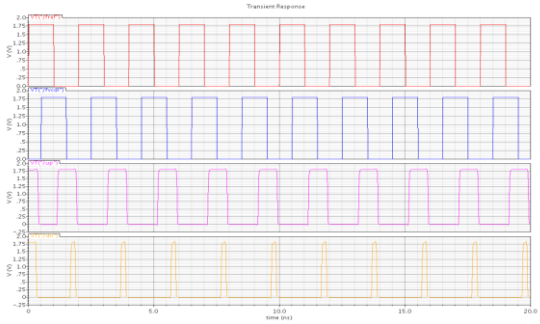

Fig-10- output of Conventional PFD at 500 MHz

(2)

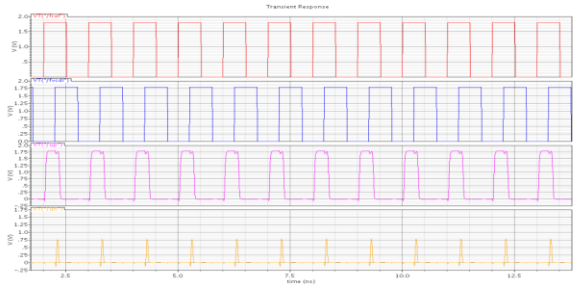

Fig. 11- output of pre-charge type PFD at 1Gbps

3.2.1.2- Charge Pump

The generation of control voltage based on DN and UP pulses are accomplished by charge pump and loop filter . The major issue with the charge pump is the equality of charging and discharging current[5]. According to the Phase Difference between the reference clock and the output phase, detected by the Phase Detector, the Charge Pump needs to charge or discharge the capacitor to increase or decrease the Control Voltage accordingly[4]. I didn't simulate this charge pump in cadence due to some unavoidable reasons with the cadence lab. But this circuit was simulated in the MATLAB, one interesting result was found. The bandwidth of the low pass filter was required to be 10 times the reference frequency. The reason is that the reference signal is square wave. It includes many sinusoidal signals having frequencies in harmonics. To get the output square, the filter must have bandwidth which allows to pass harmonics of the sinusoidal generating the square wave.

From the dynamics of DLL discussed in the chapter 2, we have got the relationship among the C1 and I1(fig-12). According to the relation we have

$$(Ip*Kvcdl)/(2pi*C1)<Wref/10.$$

We want to generate 2 Gbps signal with 8 phases , hence we need 500MHz input clock signal so that ir can generate 2 Gbps output clock, putting Wref=2*pi*500*10^6, we get

Ip/C1<1.61796*10^19

Value of Kvcdl is taken of the order of 10^(-10). We will see in our VCDL discussion, Kvcdl is coming of this order. The value of C1 is chosen of the order of fF(femto Farad) and current was in uA(micro Ampere). If we try to satisfy the required condition, we find it is always satisfying. The schematic of Charge Pump used in the project is given below (fig-13). The charging and discharging current sources are generated with help of current mirror circuits. The W/L ratio of different transistors, Ip and C1 values are given below-

(W/L)1=(W/L)2= 240nm/180nm

(W/L)3=480nm/180nm

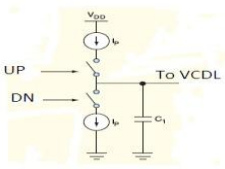

Fig. 12.Chrge Pump

The PFD has generated Up signal but PMOS is used as the switch for charging period, it requires inverted logic for operating the switches properly. The circuit given in the fig-14 is used for the generation of up_bar signal. The width of PMOS and NMOS of the inverter is set to be 2um and 1um respectively (higher width to obtain less delay).Before going to use this circuit in DLL, it was simulated alone to check its functionality. During checking, certain characteristics were kept in mind. The first thing was if only up pulse is active and down is very little or negligible, the generated control voltage must be increasing during charging but during discharging it should be constant. Similarly, if the down pulse is active then the control voltage should decrease regularly with the arrival of down pulses. In the following fig-15, the up signal was taken as high T/4 time period and down was T/10 of the period. It can be observed, during charging the control voltage is increasing while during discharging pulse, it is flat.

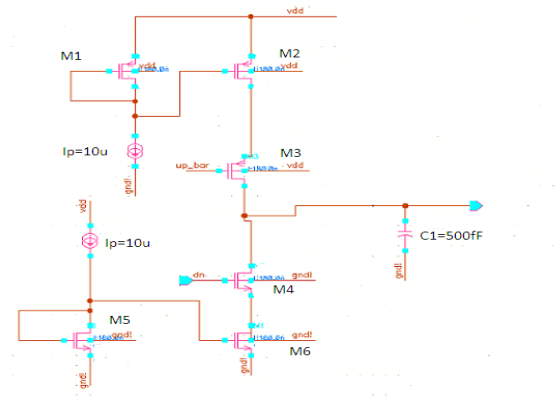

Fig-13. Schematic of Charge pump

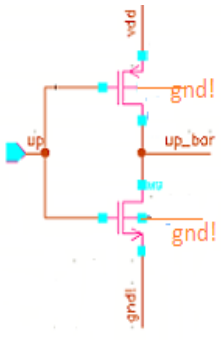

Fig-14- Inverter for up_bar generation

(W/L)4=240nm/180nm.

(W/L)5=(W/L)6=240nm/480nm.

Ip=10uA.

Cp=500fF.

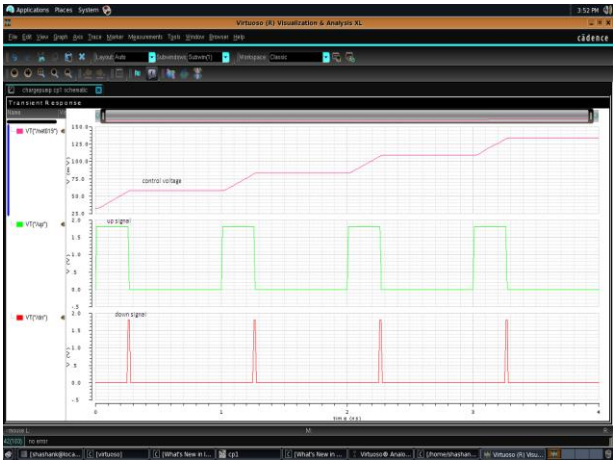

Fig-15- Response of CP

The C1 is playing a very important role for deciding charging and discharging of the control voltage. If the value of C1 is less enough, the discharging is also more and the response deviates from the desired one. Even the discharging pulse is very less, the significant decrease in control voltage can be observed. The fig-16 demonstrates it. Here C1 was taken as 10fF only but current was kept same as previous case. From the figure it is quite evident that discharging is also large which must be avoided.

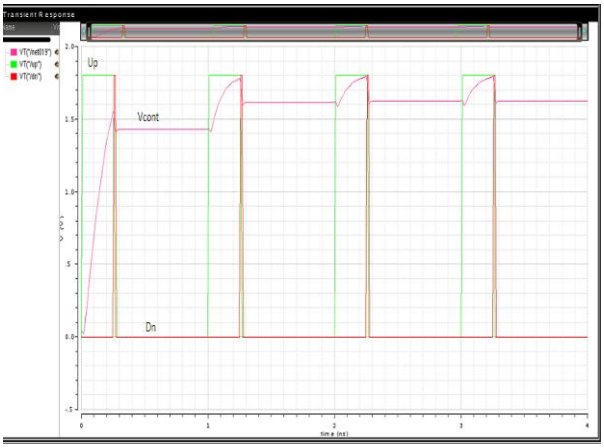

Fig.16- CP_response@10fF capacitor

The impact of Ip was observed. Control voltage is strongly dependent on the selection of charging (discharging) current. The dependence was observed and tabulated in table no 2. It is evident as much high Ip will be chosen the amount of charge on the capacitor C1 will be more and more. As the supply is 1.8V, the capacitor voltage can't go beyond this limit. This is why after 9-10uA, the increase in control voltage becomes less. As the input clock is having 2ns time period, the capacitor C1 gets charged to very large value if the current is more than 10uA. Here, Ip=10uA is used for the control voltage generation. Suppose 10mA is chosen for the

current and up signal is high for T/4=0.5ns. In this case the control voltage will go upto 10V which is imparactical here.

The impact of C1 is also significant as we have seen in the previous figure. It was tabulated in table no-3. As the capacitance value increases the generated control voltage decreases. It is very important degree of freedom during locking of DLL. When we will desire to increase the delay by some amount we can tune the value of capacitor to achieve the required control voltage which may help us in locking the DLL. During the complete simulation of the DLL , it will be quite obvious. Here one more important is initial voltage provided to control signal. As we know transistor required some value to respond properly. The project also needs such a value on the control line path. When all the smaller blocks will be connected and simulated together, we will discuss about it. Now we won't discuss this issue now but it is better to be prepared such situation.

3.2.1.3 Voltage Controlled Delay Line

It consists of delay elements. Each delay element provides T/2N amount of delay where T is the period reference signal and 2N represents the total nos. of stages implemented[6]. As we already discussed, the output of VCDL must align with the second pulse of incoming signal. The second major issue is static phase error. The PFD resolution and inequality in charging and discharging current of CP are major contributor to this problem. The static phase error is shown in fig 13. We see even each stage is providing the equal amount of delay the final phase is not aligned with the input phase[10]. Such issue generates huge amount of jitter. The design of VCDL must be done to minimize such error.

Lock range is another important characteristic of VCDL. The required range is expected as large as possible. Larger lock range allows faster locking as well as larger frequency range can be locked[25]. The project has to generate 8 phases with the help of 8 delay element. The 8 phases are sent to logic blocks which combines to produce 4 times faster clock in comparison to the input clock. This can be realized in the fig-17. 8 stages are used to generate 8 different phases. As all delay elements are similar, the delay provided by each one will be same. As for locking only the phase 8 or vcdl_out is required but for the dll_out all the 8 phases are required. The logic block needs all the 8 shifted version of the input clock. The input clock has period of 2ns , if the perfect locking is required, each stage should provide 2/8 ns delay. It means the every phase will be delayed by this value with respect to the previous phase. The delay element is controlled by the control voltage.

Table No-2

Control Voltage Vs Ip

Charging/Discharging Current Ip (uA)	Control Voltage (volts.)
2	0.712
3	0.824
4	0.971
5	1.615
6	1.375
7	1.462
8	1.513
9	1.549
10	1.551
100	1.675
1000	1.751

Table No-3

Control Voltage Vs C1

Capacitor Value C1(fF)	Control Voltage(V)
500	1.55
600	1.51
700	1.42
800	1.3
900	1.1

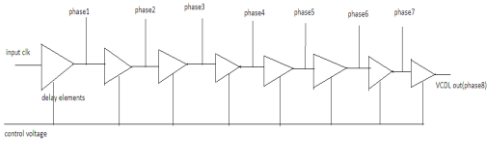

Fig-17- delay stages of VCDL

Now we discuss about the individual delay element. We can expect the delay must be variable. As the control voltage changes the delay varies. The fig 18 shows one of the delay stages used in the VCDL circuit. The control voltage is applied M2 ,M4 and M6 directly. The control signal for PMOS devices are obtained by connecting M1 as diode connected load. As we want to have variable delay so the resistance offered by current starved transistors should vary with the applied voltage. To obtain such functionality the transistors M3, M4,M5 and M6 are biased in the triode region. As the control voltage changes the resistance offered by these transistors also changes and that allow variable current to the chain of the inverters. As even no of inverters are used, the delay element does not provide any phase change. It is for delay only. While simulating the

circuit, the kick-back effect is observed due to capacitances of M2,M4 and M6. This was distorting the signals. To avoid it , control signal can be sent using current mirror circuit. It is shown in fig-19. The transistors are used in current mirror fashion to get the same current in the other branch of the circuit. The W/L ratios of all the transistors are kept same. The current generated by Vcont-in in M3 is mirrored via M1 to other branch. The diode connected nmos load will produce the voltage that is equal or nearly equal to the original control voltage produced by the charge pump.It must satisfy the condition that the Vcont_out should be equal or nearly equal to Vcont_in. It was simulated and tabulated in table no-4.

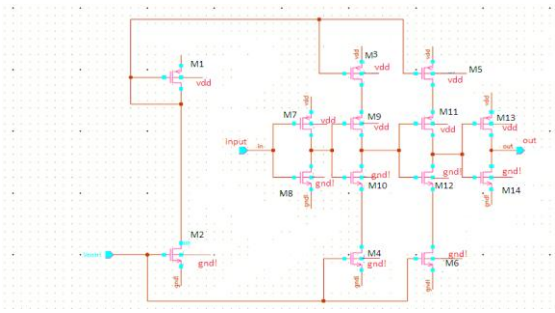

Fig- 18 schematic of delay element

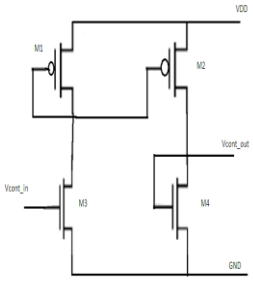

Fig-19 Circuit to avoid kick back

Table No- 4

Vcont_out Vs Vcont_in

Vcont_in(v)	Vcont_out(v)
0.4	0.45
0.5	0.54
0.6	0.63
0.7	0.72
0.8	0.81
0.9	0.89
1.0	0.96
1.1	1.03
1.2	1.07
1.3	1.11
1.4	1.14
1.5	1.16
1.6	1.17

We can observe, the output of the kick-back avoiding circuit is almost same as input voltage in the region of interest. When the input was below 0.4v transistor M3 was in cut-off. It started to operate in saturation when input control voltage reaches 0.5v. When the input control goes beyond 1.1v the output control voltage starts to deviate from the value of the input control voltage. Hence , the Kvcdl must be calculated before 1v control voltage.

Now we should concentrate on the delay provided by the delay stages. The delay observed when the control voltage was varied. It is tabulated in table no 5 given below. We can observe, as the control voltage increases the resistance of the transistors(M3-M6 in fig-18) decreases. It allows the generation of more and more current in the inverters which lowers the delay. As we know the basic requirement was to keep the current starved transistors in the linear region, it needs to reduce the range of voltages used for the operation. Table 5 indicates, we should work near vcontrol=0.9v, similar conclusion we did while observing the vcont_out vsvcont_in(table no-4). The Kvcdl is not a constant quantity as the slope of delay vsvcont is not linear. Hence we will calculate the Kvcdl only near vcont=0.9v which is going to be used for the simulation. The fig-20 can be referred to calculate Kvcdl. It shows the approximate nature of the delay vs control voltage.

Magnitude of Kvcdl= (227-176)/(1.0-0.9)

=510ps/v

As the target output speed of the clock is 2Gbps and the input clock frequency is 500MHz, it would be interesting to find the control voltage at which the loop is going to locked. During simulation it was found to be vcont should be 0.9v. It gives some idea regarding the required control voltage in locked state. Fig-21 shows the required delay of the input signal which aligns the second pulse of the input clock with the final phase of vcdl.

Table No-5

Delay of a single stage Vs Vcont

Control Voltage(V)	Delay of one stage(ps)
0.6	875
0.7	449
0.8	296
0.9	227
1.0	176
1.1	147
1.2	145
1.3	143
1.4	148
1.5	151
1.6	146
1.7	147

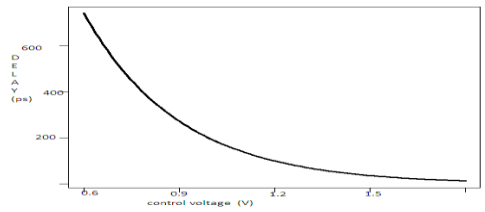

Fig-20 chracteristics of delay vs control voltage

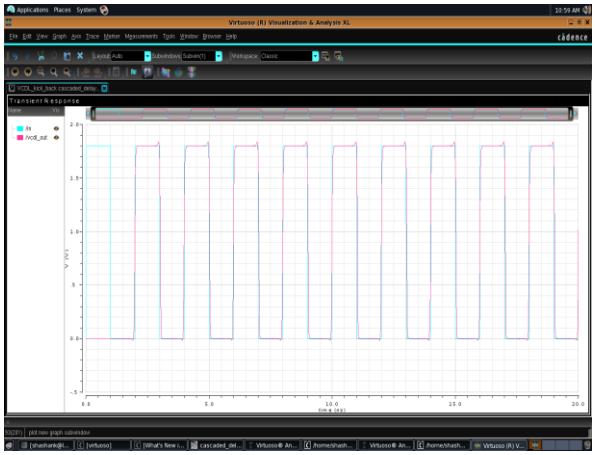

Fig-21 required alignment of vcdl_out and Clk_input @ vcont=0.9v

3.2.1.4 Logic Block

Now we have reached in the final stage of the CMU operation. The logic block combines the different phases produced by VCDL. The working principle is the each odd phase is logically ANDed with the complement of succeeding even phase and all the outputs of the AND gates are logically ORed to produce the output which shows clock of 4 times the frequency of the input.

Before sending the phases of VCDL to logic block , buffering is required. As even phases should be inverted, it can be sent using the chain of inverters. The odd phases should also be buffered so even no of inverters can be used. Fig-22 and fig-23 illustrate the current discussion. Now question arises why transmission gate is used. As we know, the correct output of DLL is completely dependent upon the delay of the phases. The phases coming out of VCDL must not touch in any way. As in non-inverting buffer 4 transistors are utilized and in inverting buffer 3 inverters are used, there would be delay mismatch if the path delay is not equated. Transmission is designed in such a way that it gives delay equal to one inverter.

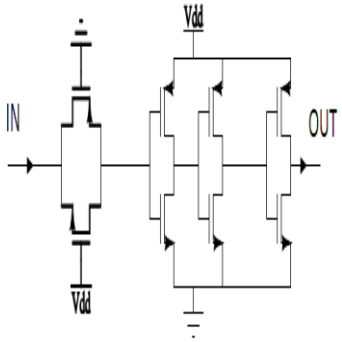

Fig-22 Inverting buffer

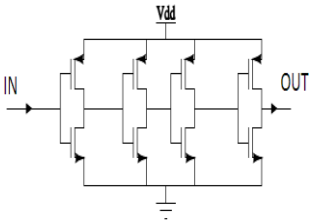

Fig-23 Non-inverting Buffer

The OR gate and AND gate are shown in fig-24 and fig-25 respectively. We may wonder how such operations in logic block can generate the multiplied frequency clock. To illustrate it we can refer fig-27. Here only four phases are considered to save time and space. The 2 nos. of AND gated are used for combining the odd and even phases. 2 nos. of OR gates are used to combine the outputs of AND gates. We can use 4 input OR gate also but the here 2 input OR gate is used two times (in the project, not in the example). The procedure of multiplication is very much evident from the diagram shown. Similarly 8 phases are used in the project. As per requirement 4 nos of AND and 2 nos. of OR are used to get the multiplication of 4 of the input frequency. The path delay provided by these gates is not so much important now because all signals are passing through similar path.

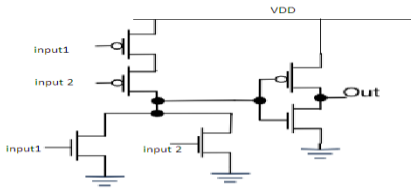

Fig.24- OR gate

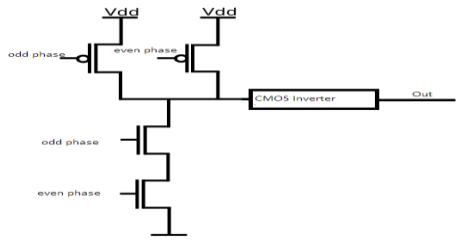

Fig-25 AND gate

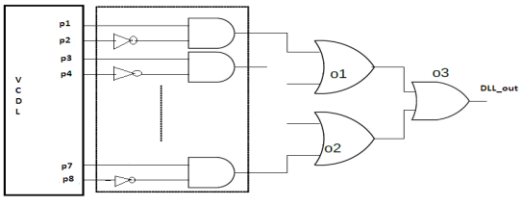

Fig- 26 Logic Block

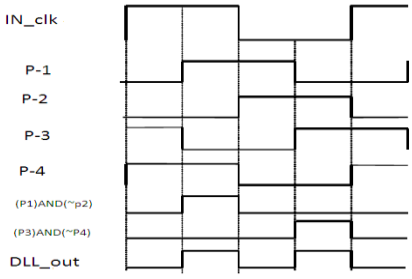

Fig-27 frequency multiplication (demo)

For the verification of the operation , logic block was simulated separately. The input clock was assumed having frequency 500MHz. Hence duration of the pulse is 2ns , the 8 phases of VCDL were taken directly from the source having initial delay of 250ps, 500ps, 750ps, 1000ps, 1250ps, 1500ps,1750ps and 2000ps respectively. These signals were fed to the logic block. The even signals were passed through the inverting buffer while the odd phases were passed through the non-inverting buffers. We can refer to fig- 28. The output clock can be observed. It has four times more frequency than the input clock. The alignment is not in the figure. It is not important because we are not going to use the input clock anywhere. Our interest was in output clock which must be 4 times as fast as the input clock. It is obtained. It will be sent to the serializer system. As serializer will need 3 different types of clock speed(2Gbps, 1Gbps, 500MHz), divider circuit will be used for the division of the frequency. Now we need to concentrate on the simulation of DLL including all the blocks. Individual block- simulation is not enough to assure the correct working of the overall unit. There are so many factors, we need to keep in mind.

Fig-28 output of logic block

VI. CONCLUSION

The improvement in device characteristics and signal processing modules can be cashed by increasing the speed of interfacing circuits used between different chips. The serial communication has distinct advantages over parallel communication. Serializers based on CMOS and CML both should be utilized properly to take the advantages of high speed as well as lower power consumption. CMU based on DLL concept is a very useful technique to get high frequency clock. DLL has different components which put stringent limitations on the performance of the CMU. The resolution of PFD must be enhanced to get less static phase error. The main culprit of poor performance of PFD is delay in feedback path. In this regard pre-charge type PFD offers less delay in comparison to conventional PFD. This is why pre-charge type PFD is preferable.

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